CHANDIGARH ENGINEERING COLLEGE- CGC, LANDRAN, MOHALI

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT

Assignment No: 1

Subject and Subject code: Digital System Design BTEC– 302-18
Semester: 3rd
Date on which assignment given: 5-09-2022
Date of submission of assignment: 12-09-2022

Note: Each question carries 2 marks **Total marks: 10**

Course Outcomes

CO 1	Apply concepts of Boolean algebra for handling logical expressions.
CO 2	Understand working and realization of combinational logical expressions.
CO 3	Understand working flip-flops and use them in designing of sequential circuits.
CO 4	Understand fundamental concepts of logic families and architectural of programmable devices.
CO 5	Use HDL programming tool for simulation of combinational and sequential circuits

Bloom's Taxonomy Levels

L1 – Remembering, L2 – Understanding, L3 – Applying, L4 – Analyzing, L5 – Evaluating, L6 - Creating

S. No.	Questions	Relevance to CO No.	Bloom's Level
1.	Design the Half adder using NAND Gate.	CO2	L6
2.	Implement the 4 bit binary to gray code convertor (using K-map for each output).	CO2	L3
3.	Implement the all logic gate (AND, OR, NOT, NAND, Ex-OR, EX-NOR) using NOR gate only.	CO1	L3
4.	Convert the following number as given below (a) $(101011001)_2$ -------($)_{16}$ (b) (37.4)8----------( )10 (c) (BAD)16----------( )8 (d) (22.75)10----------( )2	CO1	L2
5.	Using Boolean identities, reduce the given Boolean expression (a) x'y'z +yz+ xz (b) (A + B' + C')(A + B' + C)(A + B + C')	CO 1	L4